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|  | **DEPARTMENT OF COMPUTER ENGINEERING** |

**Experiment No. 02**

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| Semester | S.E-Semester III – Computer Engineering |
| Subject | Digital Logic and Computer Architecture |
| Subject Professor In-charge | Prof. Avinash Shrivas |
| Assisting Teachers | Prof. Avinash Shrivas |

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| Division and Batch – Division A, Batch 1 |
| Date of Implementation – 3/08/2022 |
| Experiment Title: Realizing Basic Gates |
| **Theory:**  AND Gate  The AND gate plays an important role in the digital logic circuit. The output state of the AND gate will always be low when any of the inputs states is low. Simply, if any input value in the AND gate is set to 0, then it will always return low output (0).  The logic or Boolean expression for the AND gate is the logical multiplication of inputs denoted by a full stop or a single dot as (A.B=Y)  The value of Y will be true when both the inputs A and B are set to true.  OR Gate  The output, Q of a “Logic OR Gate” only returns “LOW” again when all of its inputs are at a logic level “0”. In other words, for a logic OR gate, any “HIGH” input will give a “HIGH”, logic level “1” output.  The logic or Boolean expression given for a digital logic OR gate is that for *Logical Addition* which is denoted by a plus sign, ( + ) giving us the Boolean expression of:  A+B = Q.  Thus, a logic OR gate can be correctly described as an “Inclusive OR gate” because the output is true when both of its inputs are true (HIGH).  NOT Gate  Inverting NOT gates are single input devicse which have an output level that is normally at logic level “1” and goes “LOW” to a logic level “0” when its single input is at logic level “1”, in other words it “inverts” (complements) its input signal.  The output from a NOT gate only returns “HIGH” again when its input is at logic level “0” giving us the Boolean expression of:  A = Q.  Then we can define the operation of a single input digital logic NOT gate as being:    “If A is NOT true, then Q is true” |
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| **Implementation**  **AND Gate** Diagram  Description automatically generated  Truth Table  A picture containing table  Description automatically generated  **OR GATE**  Diagram  Description automatically generated  Truth Table  Box and whisker chart  Description automatically generated with low confidence  **NOT GATE**  Chart, line chart  Description automatically generated  Truth Table  Chart  Description automatically generated |
| Conclusion: In this experiment we understood the working of AND, OR and NOT gates  AND gate - If any input value in the AND gate is set to 0, then it will always return low output (0).  OR gate - If any input value in the OR gate is set to 1, then it will always return High output (1).  NOT gate - if any input value in the NOT gate is set to 0, then it will always return 1. And vice versa |